AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) A durable chip pad comprising:
   a terminal metal layer disposed on a passivating layer;
   a diffusion barrier layer on said terminal metal layer;
   a conducting layer pad on said diffusion barrier;
   a hard test barrier layer on, and enclosing, said conducting layer pad; and
   a plate passivating layer on said hard test barrier layer.

2. (original) A durable chip pad as in claim 1, wherein said diffusion barrier layer includes an adhesion layer on barrier metallurgy.

3. (original) A durable chip pad as in claim 2, wherein said barrier metallurgy is selected from a group of metals and metal alloys comprising titanium (Ti), titanium nitride (TiN), titanium tungsten (TiW), chromium (Cr) and tantalum/tantalum nitride (Ta/TaN).

4. (original) A durable chip pad as in claim 3, wherein said adhesion layer is selected from a group of metals and metal alloys comprising chrome-copper (CrCu), nickel vanadium (NiV) and titanium (Ti).

5. (previously presented) A durable chip pad as in claim 1, wherein said plated hard test barrier layer comprises a nickel (Ni) layer.

6. (canceled)

7. (original) A durable chip pad as in claim 1, wherein said plate passivating layer is selected from a group of metals comprising copper (Cu), ruthenium (Ru), rhodium (Rh) and gold (Au).

8. (previously presented) An integrated circuit (IC) chip with circuits formed thereon, a plurality of chip interconnect pads formed on a surface of said IC chip, one or more of said plurality of chip interconnect pads being a durable chip pad comprising:

a terminal metal layer disposed on a chip passivating layer and connecting to underlying chip wiring through a via through said chip passivating layer;

an adhesion/barrier layer on said terminal metal layer;

a seed pad on said adhesion/barrier layer;

a hard test barrier layer plated on, and enclosing, said seed pad; and

a plate passivating layer on said hard test barrier layer.

9. (previously presented) An IC as in claim 8, wherein said adhesion/barrier layer includes an adhesion layer on barrier metallurgy and said barrier metallurgy is selected from a group of metals and metal alloys comprising titanium (Ti), titanium nitride (TiN), titanium tungsten (TiW), chromium (Cr) and tantalum/tantalum nitride (Ta/TaN).

10. (original) An IC as in claim 9, wherein said adhesion layer is selected from a group of metals and metal alloys comprising chrome-copper (CrCu), nickel vanadium (NiV) and titanium (Ti).

11. (previously presented) An IC as in claim 10, wherein said seed pad comprises a copper pad.

12. (currently amended) An IC as in claim 11, wherein said hard test barrier layer comprises a nickel (Ni) layer plated to and extending ~~extends~~ along the sides said copper pad.

13. (original) An IC as in claim 12, wherein said plate passivating layer is selected from a group of metals comprising copper (Cu), ruthenium (Ru), rhodium (Rh) and gold (Au).

14. (original) An IC as in claim 13, wherein said IC is one of a plurality of identical ICs on a wafer, each of said plurality of identical ICs located in a die on said wafer.

15 – 20 (canceled)

21. (currently amended) A durable chip pad comprising:

a terminal metal layer disposed on a passivating layer;

a diffusion barrier layer on said terminal metal layer;

a copper seed layer pad on~~, and enclosing,~~ said diffusion barrier layer;

a nickel layer plated to, and enclosing, said copper seed layer pad; and

a plate passivating layer on said nickel layer.

22. (previously presented) A durable chip pad as in claim 21, wherein said diffusion barrier layer includes an adhesion layer on barrier metallurgy.

23. (previously presented) A durable chip pad as in claim 22, wherein said barrier metallurgy is selected from a group of metals and metal alloys comprising titanium (Ti), titanium nitride (TiN), titanium tungsten (TiW), chromium (Cr) and tantalum/tantalum nitride (Ta/TaN).

24. (previously presented) A durable chip pad as in claim 23, wherein said adhesion layer is selected from a group of metals and metal alloys comprising chrome-copper (CrCu), nickel vanadium (NiV) and titanium (Ti).

25. (previously presented) A durable chip pad as in claim 21, wherein said plate passivating layer is selected from a group of metals comprising copper (Cu), ruthenium (Ru), rhodium (Rh) and gold (Au).